FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11447-1E

MEMORY Mobile FCRAM™
CMOS

64M Bit (4 M word × 16 bit)

Mobile Phone Application Specific Memory

MB82DP04184E-65L

■ DESCRIPTION

The Fujitsu MB82DP04184E is a CMOS Fast Cycle Random Access Memory (FCRAM*) with asynchronous Static Random Access Memory (SRAM) interface containing 67,108,864 storages accessible in a 16-bit format.

This MB82DP04184E is suited for mobile applications such as Cellular Handset and PDA.

*: FCRAM is a trademark of Fujitsu Limited, Japan.

■ FEATURES

- Asynchronous SRAM Interface
- Fast Access Time : t_{AA} = t_{CE} = 65 ns Max
- 8 words Page Access Capability : t_{PAA} = 20 ns Max
- Low Voltage Operating Condition : V_{DD} = 2.6 V to 3.1 V
- Wide Operating Temperature : T_A = 0 °C to + 70 °C
- Byte Control by $\overline{LB}$ and $\overline{UB}$
- Low Power Consumption : I_{DDA1} = 40 mA Max
  I_{DDS1} = 200 µA Max
- Various Power Down mode : Sleep
  8M-bit Partial
  16M-bit Partial
- Shipping Form : Wafer, Chip, 71-ball plastic FBGA

■ MAIN SPECIFICATIONS

Parameter	MB82DP04184E-65L
Access Time (Max) (t_{CE}, t_{AA})	65 ns
Active Current (Max) (I_{DDA1})	40 mA
Standby Current (Max) (I_{DDS1})	200 µA
Power Down Current (Max) (I_{DDPS})	10 µA

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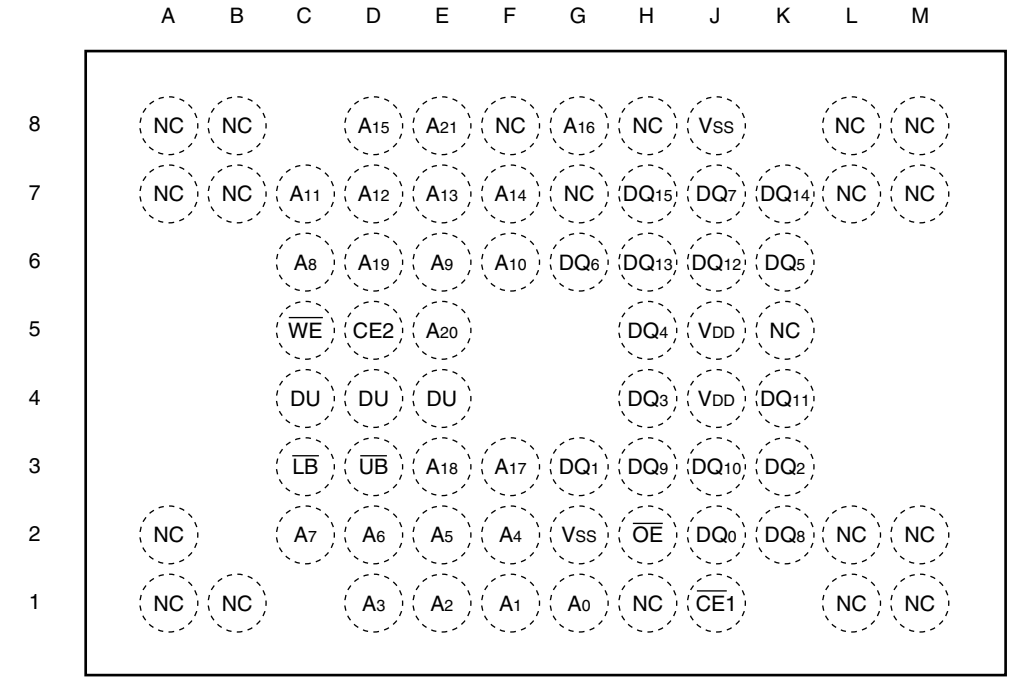
■ PIN ASSIGNMENT

(TOP VIEW)

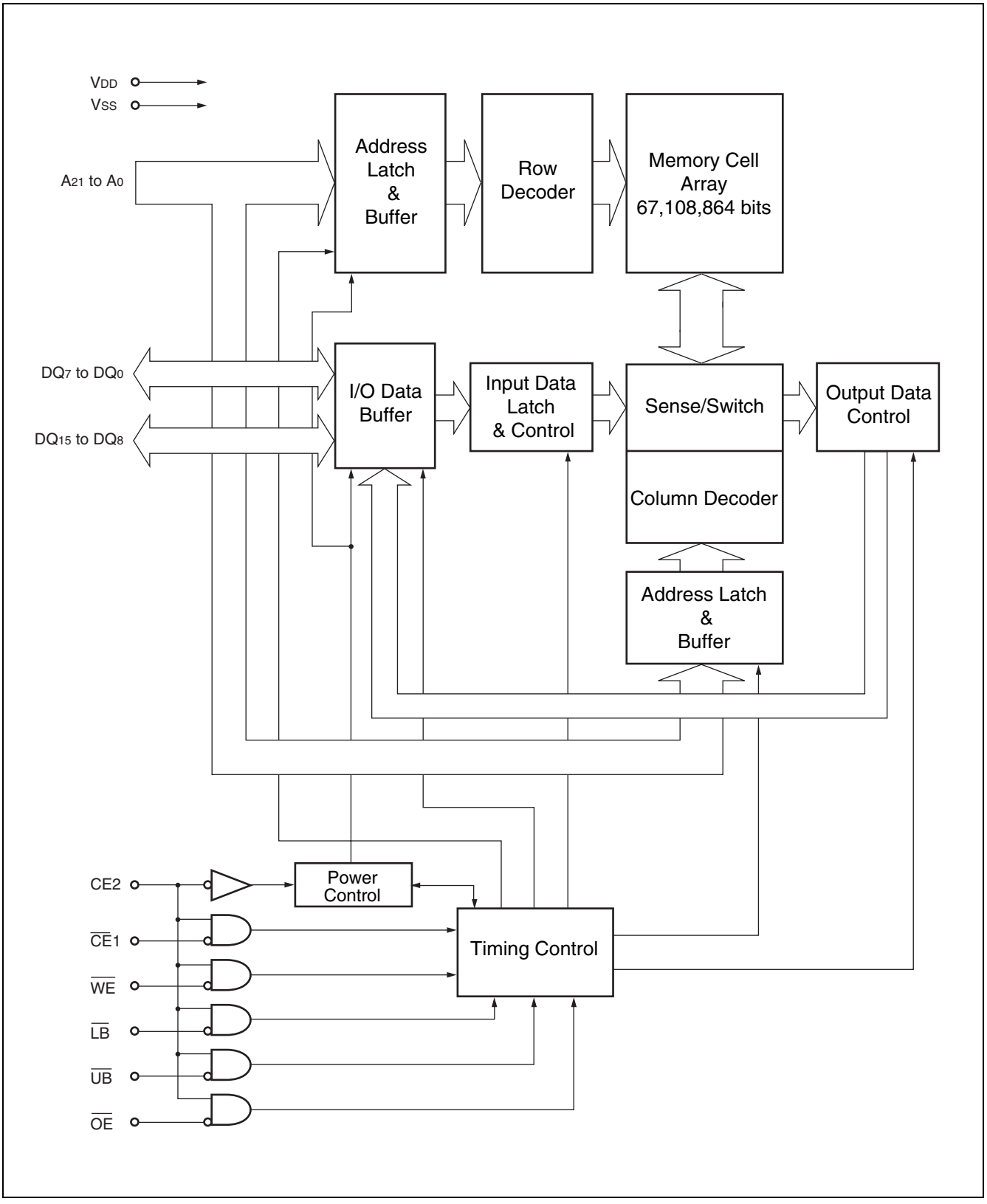


(BGA-71P-M03)

■ PIN DESCRIPTION

Pin Name	Description
A_{21} to A_0	Address Input
$\overline{CE}1$	Chip Enable 1 (Low Active)
CE2	Chip Enable 2 (High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{LB}$	Lower Byte Control (Low Active)
$\overline{UB}$	Upper Byte Control (Low Active)
DQ_7 to DQ_0	Lower Byte Data Input/Output
DQ_{15} to DQ_8	Upper Byte Data Input/Output
V_{DD}	Power Supply Voltage
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



■ FUNCTION TRUTH TABLE

Mode	CE2	$\overline{CE1}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	A_{21} to A_0	DQ_7 to DQ_0	DQ_{15} to DQ_8
Standby (Deselect)	H	H	X	X	X	X	X	High-Z	High-Z
Output Disable*1	H	L	H	H	X	X	*3	High-Z	High-Z
Output Disable (No Read)			H	L	H	H	Valid	High-Z	High-Z
Read (Upper Byte)					H	L	Valid	High-Z	Output Valid
Read (Lower Byte)					L	H	Valid	Output Valid	High-Z
Read (Word)					L	L	Valid	Output Valid	Output Valid
No Write			L	H*4	H	H	Valid	Invalid	Invalid
Write (Upper Byte)					H	L	Valid	Invalid	Input Valid
Write (Lower Byte)					L	H	Valid	Input Valid	Invalid
Write (Word)					L	L	Valid	Input Valid	Input Valid
Power Down*2	L	X	X	X	X	X	X	High-Z	High-Z

Note : L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, High-Z = High impedance

*1 : Should not be kept this logic condition longer than 1 μs.

*2 : Power Down mode can be entered from standby state and all DQ pins are in High-Z state.
Data retention depends on the selection of Power Down program. Refer to "■ POWER DOWN" for the detail.

*3 : Can be either V_{IL} or V_{IH} but must be valid before read or write.

*4 : $\overline{OE}$ can be V_{IL} during write operation if the following conditions are satisfied;
(1) Write pulse is initiated by $\overline{CE}1$. Refer to "(12) Read/Write Timing 1-1 ($\overline{CE}1$ Control)" in "■ TIMING DIAGRAMS".
(2) $\overline{OE}$ stays V_{IL} during write cycle.

■ POWER DOWN

• Power Down

The Power Down is low power idle state controlled by CE2. CE2 Low drives the device in Power Down mode and maintains low power idle state as long as CE2 is kept Low. CE2 High resumes the device from Power Down mode.

This device has three Power Down modes, Sleep, 8M-bit Partial and 16M-bit Partial. The selection of Power Down mode can be programmed by series of read/write operation. Each mode has following data retention features.

Mode	Data Retention	Retention Address
Sleep (default)	No	N/A
8M-bit Partial	8M bits	000000h to 07FFFFh
16M-bit Partial	16M bits	000000h to 0FFFFFh

The default state is Sleep and it is the lowest power consumption but all data will be lost once CE2 is brought to Low for Power Down. It is not required to program to Sleep mode after power-up.

• Power Down Program Sequence

The program requires total six read/write operations with unique address and data. The device should be in standby mode in the interval between each read/write operation. The following table shows the detail sequence.

Cycle #	Operation	Address	Data
1st	Read	3FFFFFh (MSB)	Read Data (RDa)
2nd	Write	3FFFFFh	RDa
3rd	Write	3FFFFFh	RDa
4th	Write	3FFFFFh	FFFFh
5th	Write	3FFFFFh	Data Key
6th	Write	3FFFFFh	FFFFh

The first cycle is to read from most significant address (MSB).
The second and third cycles are to write to MSB. If the second or third cycle is written into the different address, the program is cancelled and the data written by the second or third cycle is valid as a normal write operation. It is recommended to write back the data (RDa) read by first cycle to MSB in order to secure the data.
The fourth to sixth cycles are to write to MSB. The data of fourth and sixth cycles must be “FFFFh” and data of fifth cycle are specific data key for mode selection. If the fourth to sixth cycles are written into different address, the program is also cancelled but write data may not be written as normal write operation.
Once this program sequence is performed from a Partial mode to the other Partial mode, the written data stored in memory cell array may be lost. Therefore, this program should be performed prior to regular read/write operation if Partial Power Down mode is used.

• Data Key

The data key has following format.

Mode	Data			
	DQ_{15} to DQ_2	DQ_1	DQ_0	Hexadecimal
Sleep (default)	1	1	1	FFFFh
8M-bit Partial	1	0	1	FFFDh
16M-bit Partial	1	0	0	FFFCh

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value		Unit
		Min	Max	
Voltage of V_{DD} Supply Relative to V_{SS}*	V_{DD}	− 0.5	+ 3.6	V
Voltage at Any Pin Relative to V_{SS}*	V_{IN}, V_{OUT}	− 0.5	+ 3.6	V
Short Circuit Output Current	I_{OUT}	− 50	+ 50	mA
Storage Temperature	T_{STG}	− 55	+ 125	°C

* : All voltages are referenced to V_{SS}.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Supply Voltage*1	V_{DD}	2.6	3.1	V
	V_{SS}	0	0	V
Input High Voltage *1, *2	V_{IH}	$V_{DD} \times 0.8$	$V_{DD} + 0.2$	V
Input Low Voltage *1, *3	V_{IL}	− 0.3	$V_{DD} \times 0.2$	V
Ambient Temperature	T_A	0	+ 70	°C

*1 : All voltages are referenced to V_{SS}.

*2 : Maximum DC voltage on input and I/O pins are V_{DD} + 0.2 V. During voltage transitions, inputs may overshoot to V_{DD} + 1.0 V for periods of up to 5 ns.

*3 : Minimum DC voltage on input or I/O pins are -0.3 V. During voltage transitions, inputs may undershoot V_{SS} to -1.0 V for periods of up to 5 ns.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ PIN CAPACITANCE

(f = 1 MHz, T_A = +25 °C)

Parameter	Symbol	Test conditions	Value			Unit
			Min	Typ	Max	
Address Input Capacitance	C_{IN1}	V_{IN} = 0 V	—	—	5	pF
Control Input Capacitance	C_{IN2}	V_{IN} = 0 V	—	—	5	pF
Data Input/Output Capacitance	C_{IO}	V_{IO} = 0 V	—	—	8	pF

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(Under recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test conditions		Value		Unit
				Min	Max	
Input Leakage Current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$		–1.0	+1.0	µA
Output Leakage Current	I_{LO}	$V_{SS} \le V_{OUT} \le V_{DD}$, Output Disable		–1.0	+1.0	µA
Output High Voltage	V_{OH}	$V_{DD} = V_{DD}$ Min, $I_{OH} = –0.5$ mA		2.4	—	V
Output Low Voltage	V_{OL}	$I_{OL} = 1$ mA		—	0.4	V
V_{DD} Power Down Current	I_{DDPS}	$V_{DD} = V_{DD}$ Max, $V_{IN} = V_{DD}$ or V_{SS}, $CE2 = V_{SS}$	Sleep	—	10	µA
	I_{DDP8}		8M-bit Partial	—	100	µA
	I_{DDP16}		16M-bit Partial	—	120	µA
V_{DD} Standby Current	I_{DDS}	$\overline{CE}1 = CE2 = V_{IH}$		—	1.5	mA
	I_{DDS1}	$V_{DD} = V_{DD}$ Max, $V_{IN} = V_{DD}$ or V_{SS}, $\overline{CE}1 = CE2 = V_{DD}$	$T_A \le +85$ °C	—	200	µA
			$T_A \le +40$ °C	—	100	µA
V_{DD} Active Current	I_{DDA1}	$V_{DD} = V_{DD}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1 = V_{IL}$ and $CE2 = V_{IH}$, $I_{OUT} = 0$ mA	t_{RC}/t_{WC} = Min	—	40	mA
	I_{DDA2}		$t_{RC}/t_{WC} = 1$ µs	—	5	mA
V_{DD} Page Read Current	I_{DDA3}	$V_{DD} = V_{DD}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1 = V_{IL}$ and $CE2 = V_{IH}$, $I_{OUT} = 0$ mA, t_{PRC} = Min		—	10	mA

Notes : • All voltages are referenced to V_{SS}.

- I_{DD} depends on the output termination, load conditions, and AC characteristics.
- After power on, initialization following power-up timing is required.
  DC characteristics are guaranteed after the initialization.
- I_{DDPS}, I_{DDP8}, I_{DDP16}, and I_{DDS1} might be higher for up to 600 ms after power-up or Power Down/standby mode entry.

2. AC Characteristics

(1) Read Operation

(Under recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Read Cycle Time	t_{RC}	65	1000	ns	*1, *2
$\overline{CE}1$ Access Time	t_{CE}	—	65	ns	*3
$\overline{OE}$ Access Time	t_{OE}	—	40	ns	*3
Address Access Time	t_{AA}	—	65	ns	*3, *5
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}	—	30	ns	*3
Page Address Access Time	t_{PAA}	—	20	ns	*3, *6
Page Read Cycle Time	t_{PRC}	20	1000	ns	*1, *6, *7
Output Data Hold Time	t_{OH}	3	—	ns	*3
$\overline{CE}1$ Low to Output Low-Z	t_{CLZ}	5	—	ns	*4
$\overline{OE}$ Low to Output Low-Z	t_{OLZ}	10	—	ns	*4
$\overline{LB}$, $\overline{UB}$ Low to Output Low-Z	t_{BLZ}	0	—	ns	*4
$\overline{CE}1$ High to Output High-Z	t_{CHZ}	—	12	ns	*3
$\overline{OE}$ High to Output High-Z	t_{OHZ}	—	12	ns	*3
$\overline{LB}$, $\overline{UB}$ High to Output High-Z	t_{BHZ}	—	12	ns	*3
Address Setup Time to $\overline{CE}1$ Low	t_{ASC}	–6	—	ns	
Address Setup Time to $\overline{OE}$ Low	t_{ASO}	10	—	ns	
Address Invalid Time	t_{AX}	—	10	ns	*5, *8
Address Hold Time from $\overline{CE}1$ High	t_{CHAH}	–6	—	ns	*9
Address Hold Time from $\overline{OE}$ High	t_{OHAH}	–6	—	ns	
$\overline{WE}$ High to $\overline{OE}$ Low Time for Read	t_{WHOL}	10	1000	ns	*10
$\overline{CE}1$ High Pulse Width	t_{CP}	10	—	ns	

*1 : Maximum value is applicable if $\overline{CE}1$ is kept at Low without change of address input of A_{21} to A_3.

*2 : Address should not be changed within minimum t_{RC}.

*3 : The output load 50 pF.

*4 : The output load 5 pF.

*5 : Applicable to A_{21} to A_3 when $\overline{CE}1$ is kept at Low.

*6 : Applicable only to A_2, A_1 and A_0 when $\overline{CE}1$ is kept at Low for the page address access.

*7 : In case page read cycle is continued with keeping $\overline{CE}1$ stays Low, $\overline{CE}1$ must be brought to High within 4 μs. In other words, page read cycle must be closed within 4 μs.

*8 : Applicable when at least two of address inputs among applicable are switched from previous state.

*9 : t_{RC}(Min) and t_{PRC}(Min) must be satisfied.

*10 : If the actual value of t_{WHOL} is shorter than specified minimum values, the actual t_{AA} of following Read may become longer by the amount of subtracting the actual value from the specified minimum value.

(2) Write Operation

(Under recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Write Cycle Time	t_{WC}	65	1000	ns	*1, *2
Address Setup Time	t_{AS}	0	—	ns	*3
$\overline{CE}1$ Write Pulse Width	t_{CW}	40	—	ns	*2, *3
$\overline{WE}$ Write Pulse Width	t_{WP}	40	—	ns	*2, *3
$\overline{LB}$, $\overline{UB}$ Write Pulse Width	t_{BW}	40	—	ns	*2, *3
$\overline{LB}$, $\overline{UB}$ Byte Mask Setup Time	t_{BS}	– 5	—	ns	*4
$\overline{LB}$, $\overline{UB}$ Byte Mask Hold Time	t_{BH}	– 5	—	ns	*5
Write Recovery Time	t_{WR}	0	—	ns	*2, *6
$\overline{CE}1$ High Pulse Width	t_{CP}	10	—	ns	
$\overline{WE}$ High Pulse Width	t_{WHP}	10	1000	ns	*7
$\overline{LB}$, $\overline{UB}$ High Pulse Width	t_{BHP}	10	1000	ns	*7
Data Setup Time	t_{DS}	12	—	ns	
Data Hold Time	t_{DH}	0	—	ns	
$\overline{OE}$ High to $\overline{CE}1$ Low Setup Time for Write	t_{OHCL}	–5	—	ns	*8
$\overline{OE}$ High to Address Setup Time for Write	t_{OES}	0	—	ns	*9

*1 : Maximum value is applicable if $\overline{CE}1$ is kept at Low without any address change.

*2 : The sum of actual write pulse (t_{CW},t_{WP} or t_{BW}) and actual write recovery time (t_{WR}) must be equal or greater than specified minimum t_{WC}.

*3 : Write pulse is defined from High to Low transition of $\overline{CE}1$, $\overline{WE}$, $\overline{LB}$ or $\overline{UB}$, whichever occurs last.

*4 : Applicable for byte mask only. Byte mask setup time is defined to the High to Low transition of $\overline{CE}1$ or $\overline{WE}$ whichever occurs last.

*5 : Applicable for byte mask only. Byte mask hold time is defined from the Low to High transition of $\overline{CE}1$ or $\overline{WE}$ whichever occurs first.

*6 : Write recovery is defined from Low to High transition of $\overline{CE}1$, $\overline{WE}$, $\overline{LB}$ or $\overline{UB}$, whichever occurs first.

*7 : Maximum values of t_{WHP} and t_{BHP} are applicable to Output Disable mode when $\overline{CE}1$ = L, $\overline{WE}$ = $\overline{OE}$ = H after write operation. Refer to “(7) Write Timing 2 ($\overline{WE}$ Control)” in “■TIMING DIAGRAMS”.

*8 : If $\overline{OE}$ is Low after minimum t_{OHCL}, read cycle is initiated. In other words, $\overline{OE}$ must be brought to High within 5 ns after $\overline{CE}1$ is brought to Low.

*9 : If $\overline{OE}$ is Low after a new address input, read cycle is initiated. In other words, $\overline{OE}$ must be brought to High at the same time or before the new address valid.

(3) Power Down Parameters

(Under recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
CE2 Low Setup Time for Power Down Entry	t_{CSP}	10	—	ns	
CE2 Low Hold Time after Power Down Entry	t_{C2LP}	65	—	ns	
$\overline{CE}$1 High Hold Time following CE2 High after Power Down Exit [Sleep mode only]	t_{CHH}	300	—	µs	*1
$\overline{CE}$1 High Hold Time following CE2 High after Power Down Exit [not in Sleep mode]	t_{CHHP}	70	—	ns	*2
$\overline{CE}$1 High Setup Time following CE2 High after Power Down Exit	t_{CHS}	0	—	ns	*1

*1 : Applicable also to power-up.

*2 : Applicable when Partial mode is set.

(4) Other Timing Parameters

(Under recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
$\overline{CE}$1 High to $\overline{OE}$ Invalid Time for Standby Entry	t_{CHOX}	5	—	ns	
$\overline{CE}$1 High to $\overline{WE}$ Invalid Time for Standby Entry	t_{CHWX}	5	—	ns	*1
CE2 Low Hold Time after Power-up	t_{C2LH}	50	—	µs	
$\overline{CE}$1 High Hold Time following CE2 High after Power-up	t_{CHH}	300	—	µs	
Input Transition Time	t_T	1	25	ns	*2

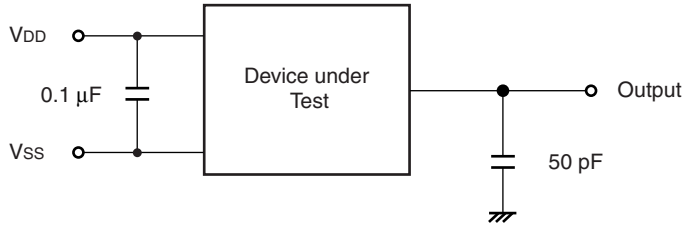
*1 : Some data might be written into any address location if t_{CHWX}(Min) is not satisfied.

*2 : The Input Transition Time (t_T) at AC testing is 5 ns as shown in below. If actual t_T is longer than 5 ns, it may violate AC specification of some timing parameters.

(5) AC Test Conditions

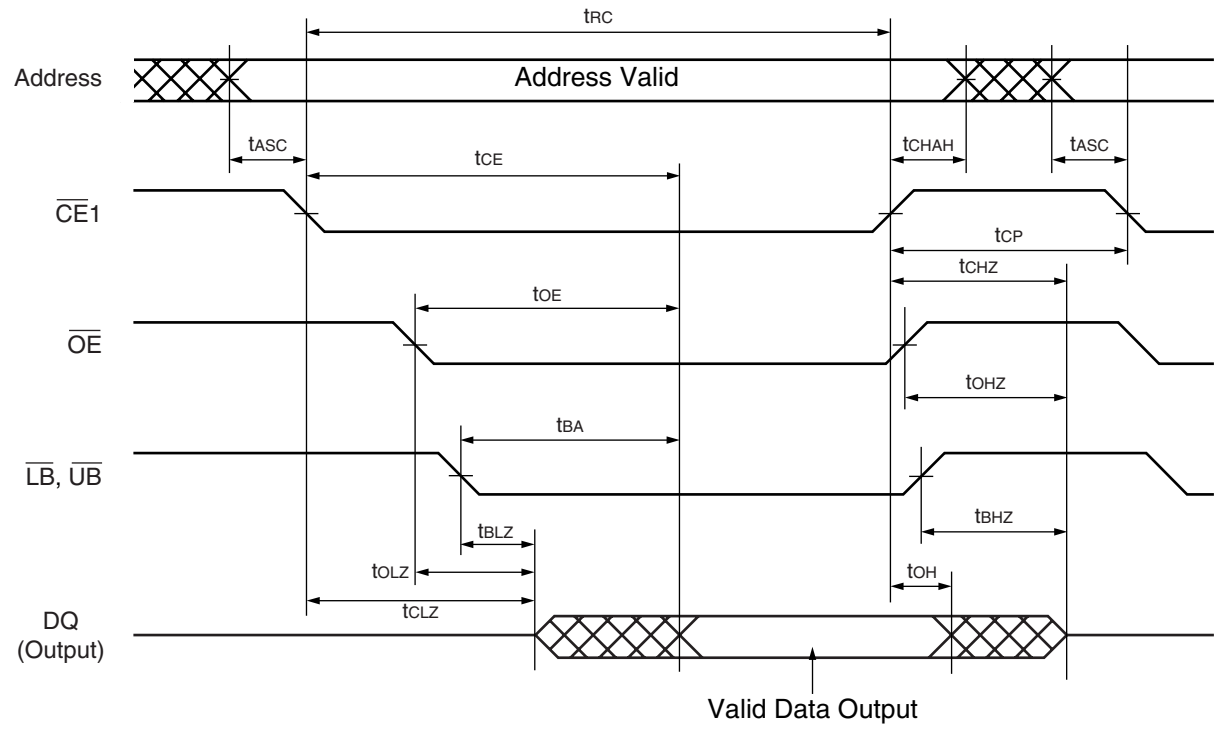
Parameter	Symbol	Test Setup	Value	Unit
Input High Voltage	V_{IH}	—	$V_{DD} \times 0.8$	V
Input Low Voltage	V_{IL}	—	$V_{DD} \times 0.2$	V
Input Timing Measurement Level	V_{REF}	—	$V_{DD} \times 0.5$	V
Input Transition Time	t_T	Between V_{IL} and V_{IH}	5	ns

- AC Measurement Output Load Circuit



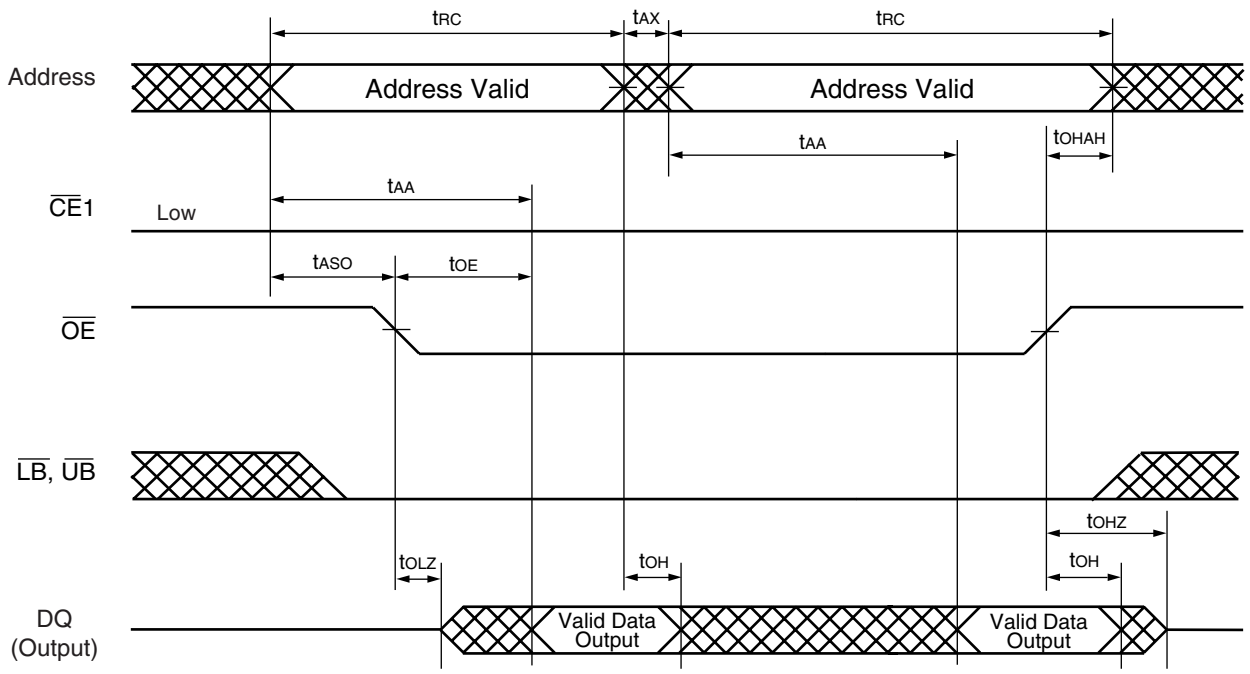
■ TIMING DIAGRAMS

(1) Read Timing 1 (Basic Timing)



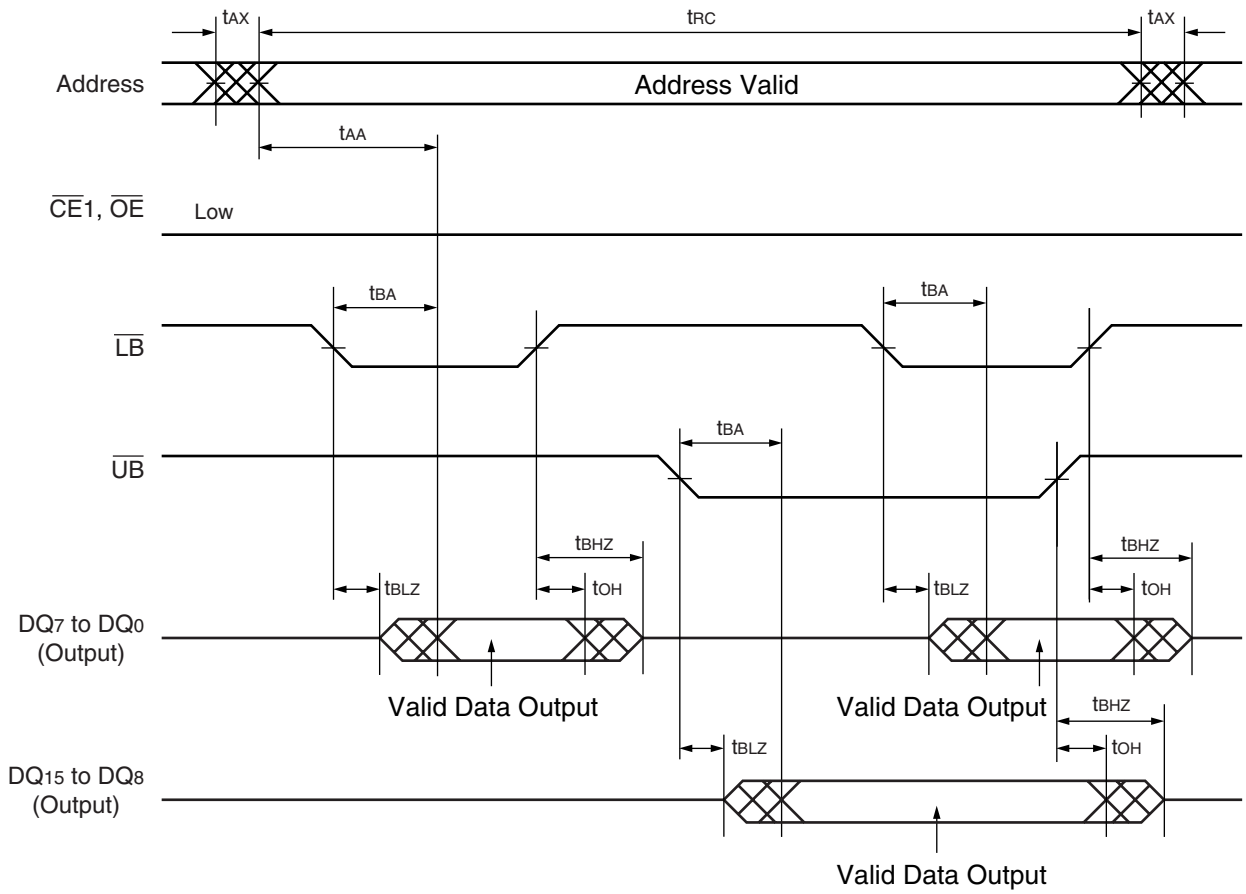
Note : This timing diagram assumes CE2 = H and $\overline{WE}$ = H.

(2) Read Timing 2 ($\overline{OE}$ Control & Address Access)



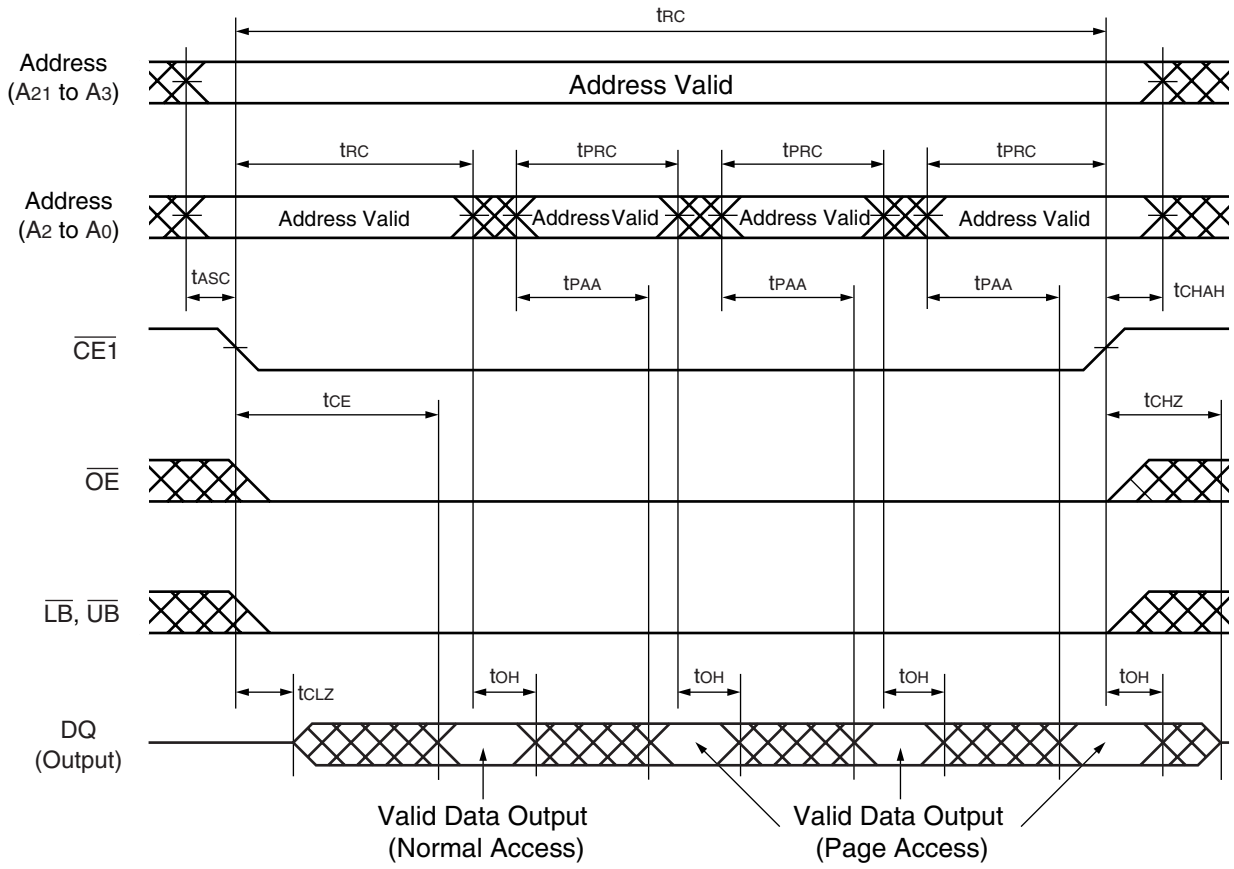
Note : This timing diagram assumes CE2 = H and $\overline{WE}$ = H.

(3) Read Timing 3 ($\overline{LB}$, $\overline{UB}$ Byte Control Access)



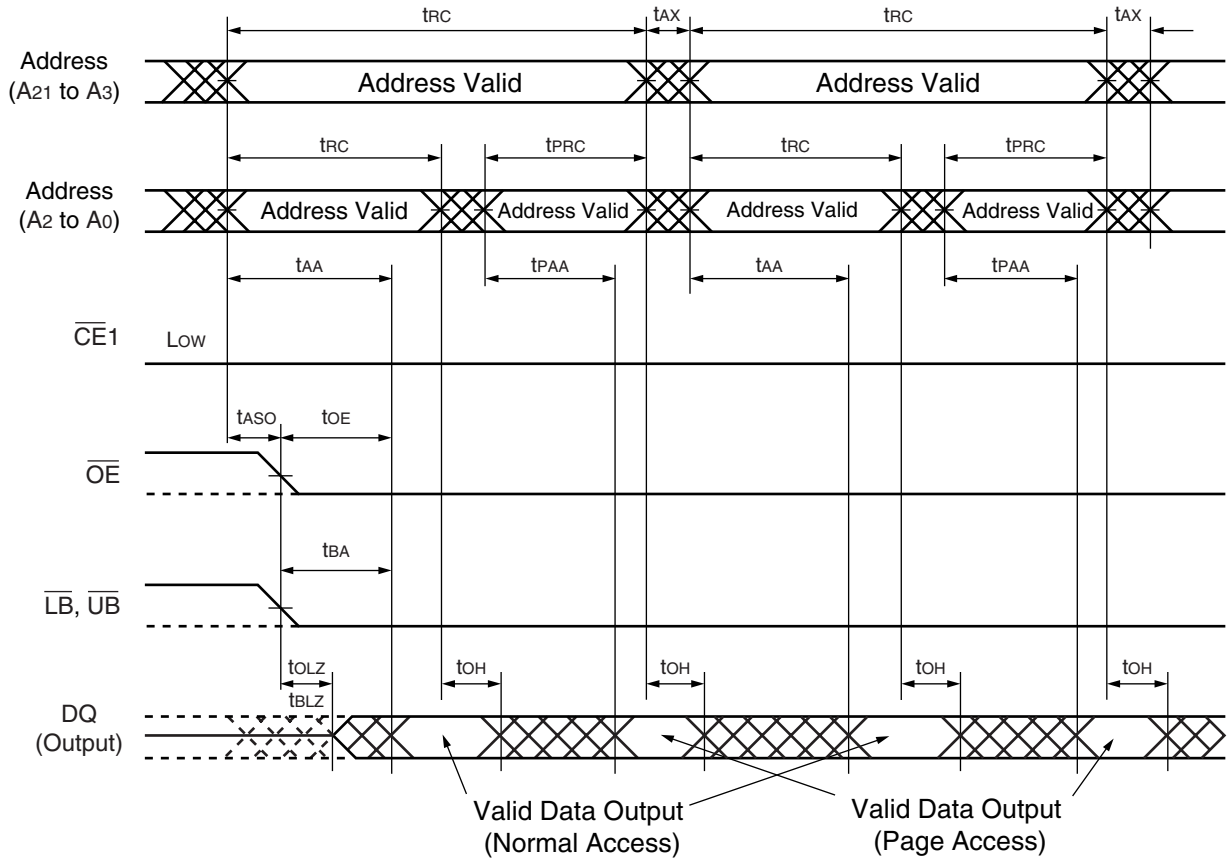
Note : This timing diagram assumes CE2 = H and $\overline{WE}$ = H.

(4) Read Timing 4 (Page Address Access after $\overline{CE}1$ Control Access)



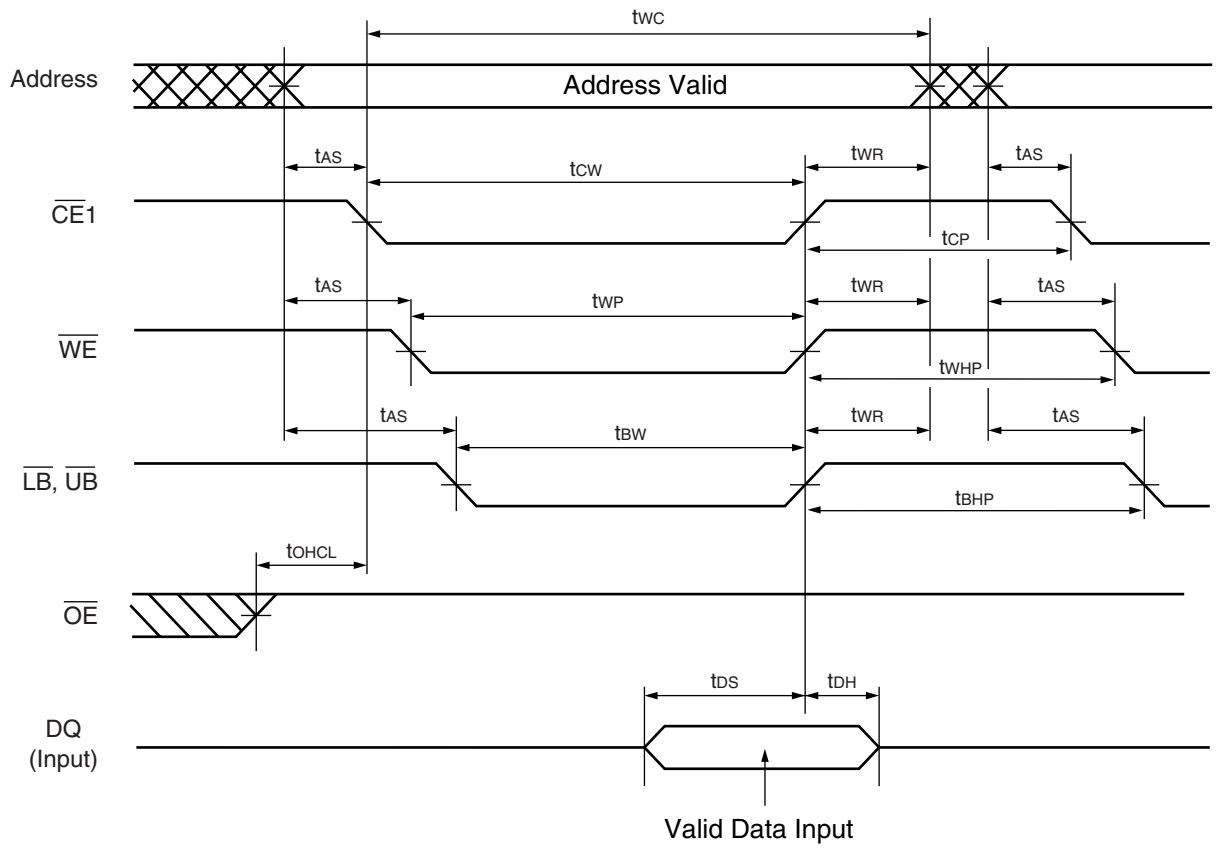
Note : This timing diagram assumes CE2 = H and $\overline{WE}$ = H.

(5) Read Timing 5 (Random and Page Address Access)



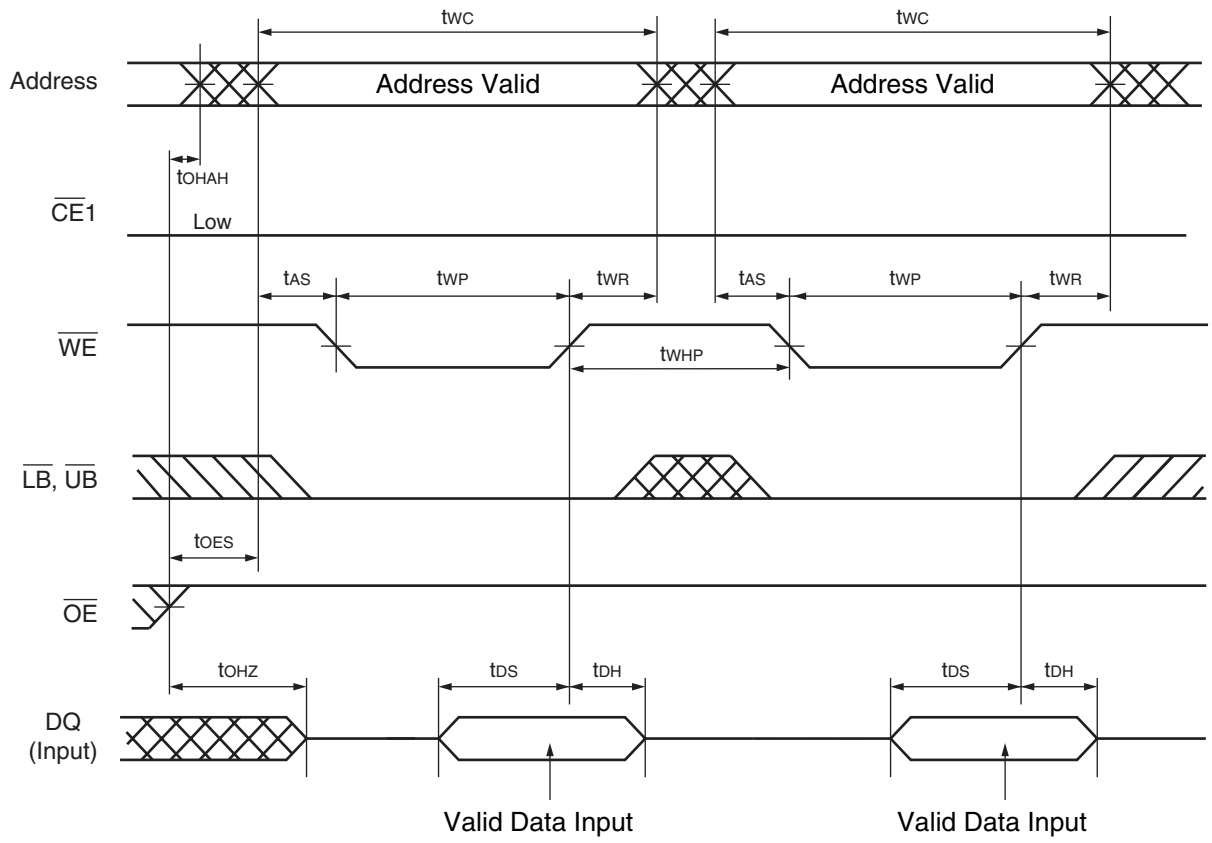
Notes : • This timing diagram assumes CE2 = H and $\overline{WE}$ = H.
• Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{CE}1$ and $\overline{OE}$ are Low.

(6) Write Timing 1 (Basic Timing)



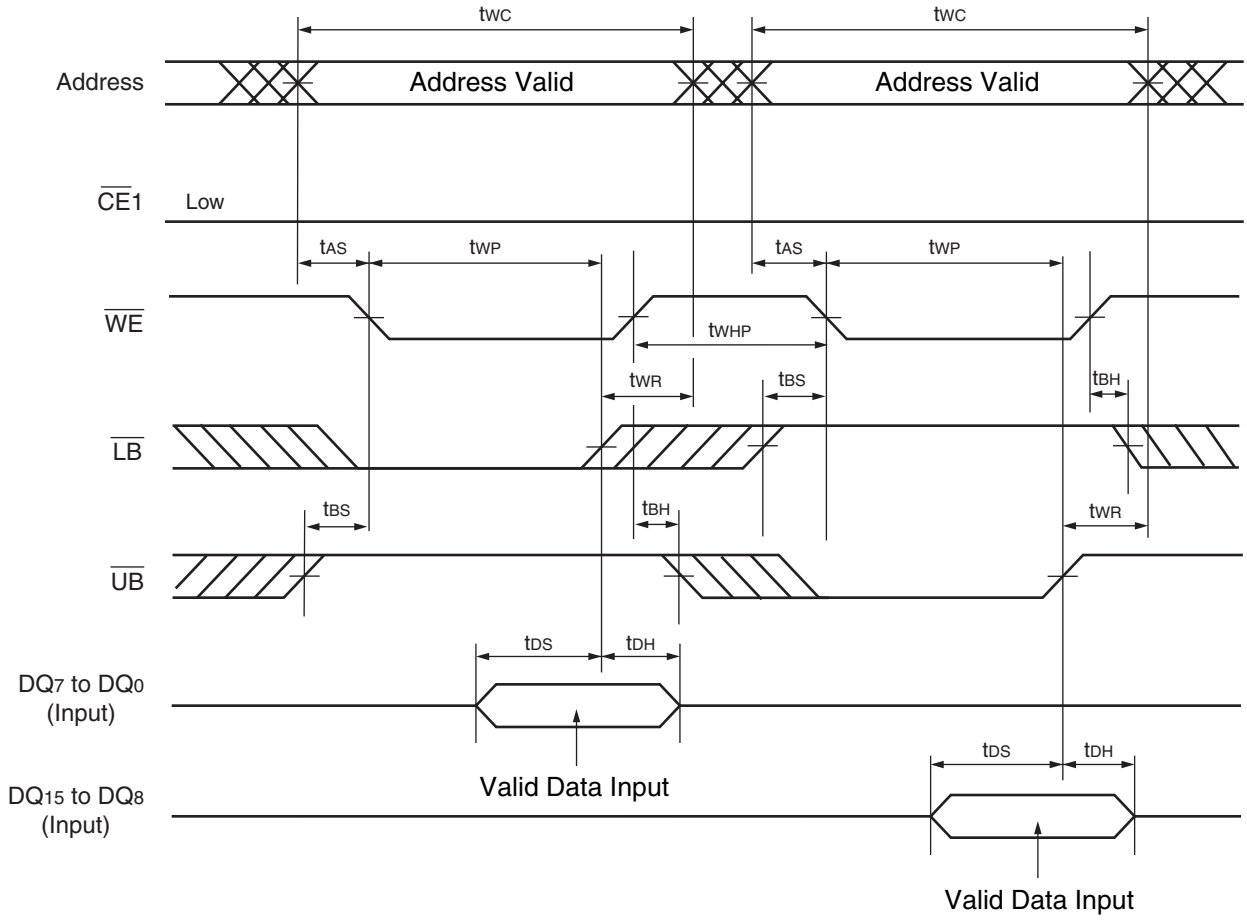
Note : This timing diagram assumes CE2 = H.

(7) Write Timing 2 ($\overline{WE}$ Control)



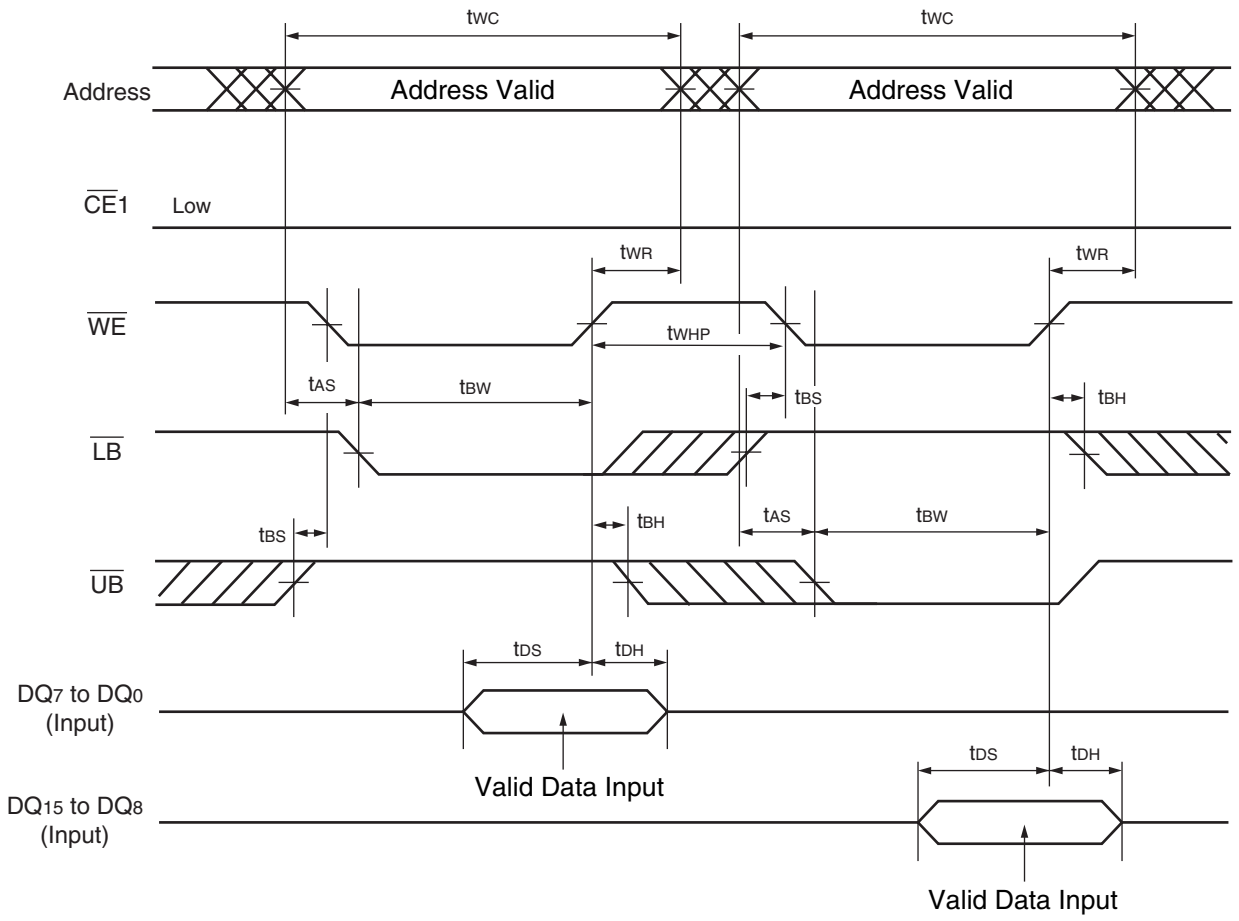
Note : This timing diagram assumes CE2 = H.

(8) Write Timing 3-1 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



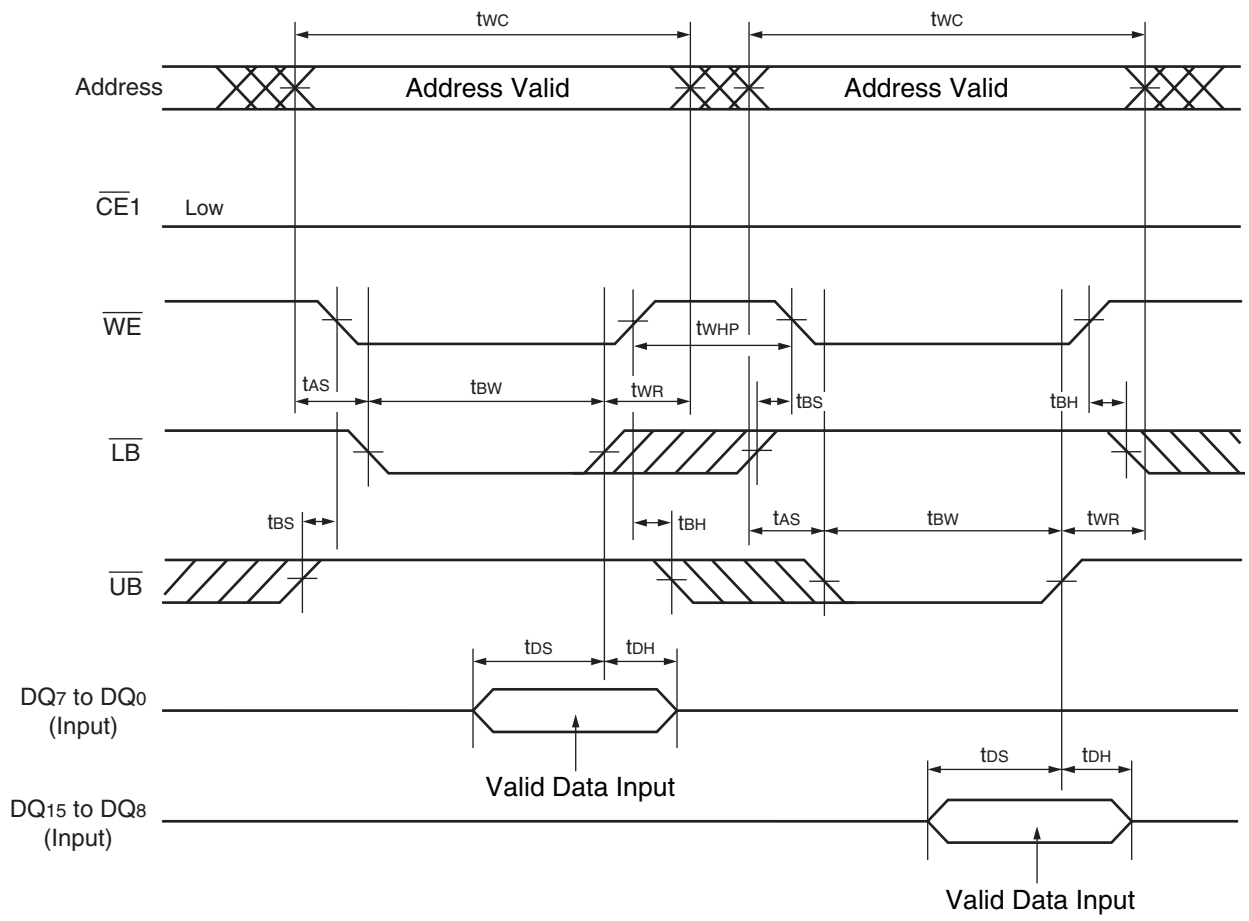
Note : This timing diagram assumes CE2 = H and $\overline{OE}$ = H.

(9) Write Timing 3-2 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



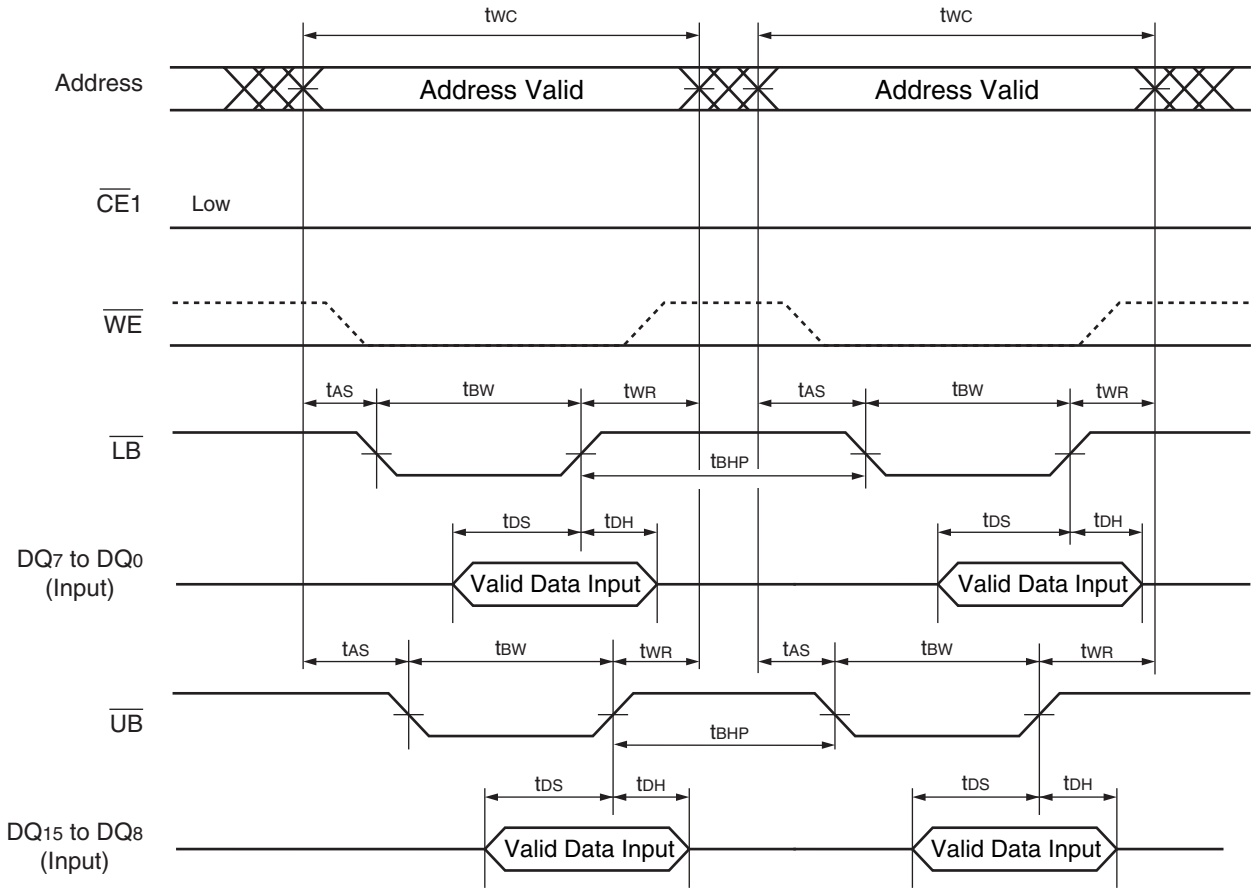
Note : This timing diagram assumes CE2 = H and $\overline{OE}$ = H.

(10) Write Timing 3-3 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



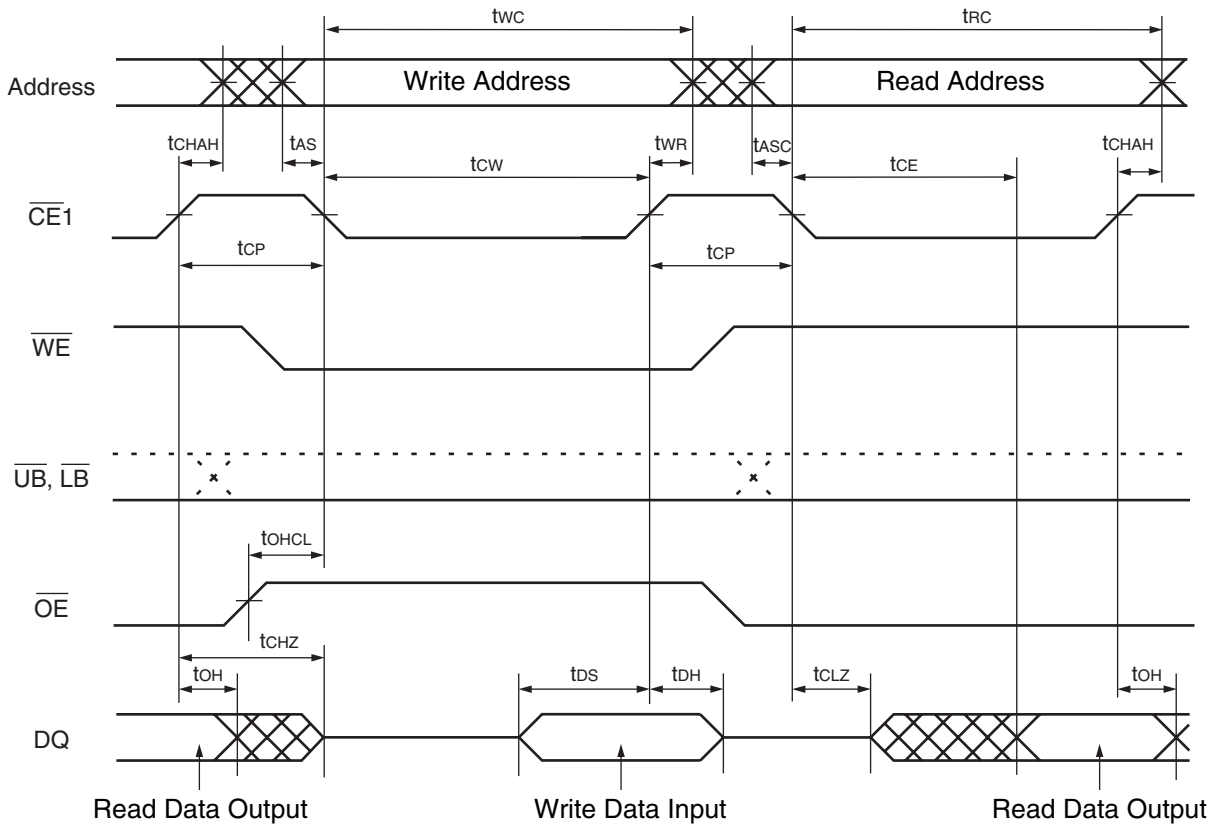
Note : This timing diagram assumes CE2 = H and $\overline{OE}$ = H.

(11) Write Timing 3-4 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



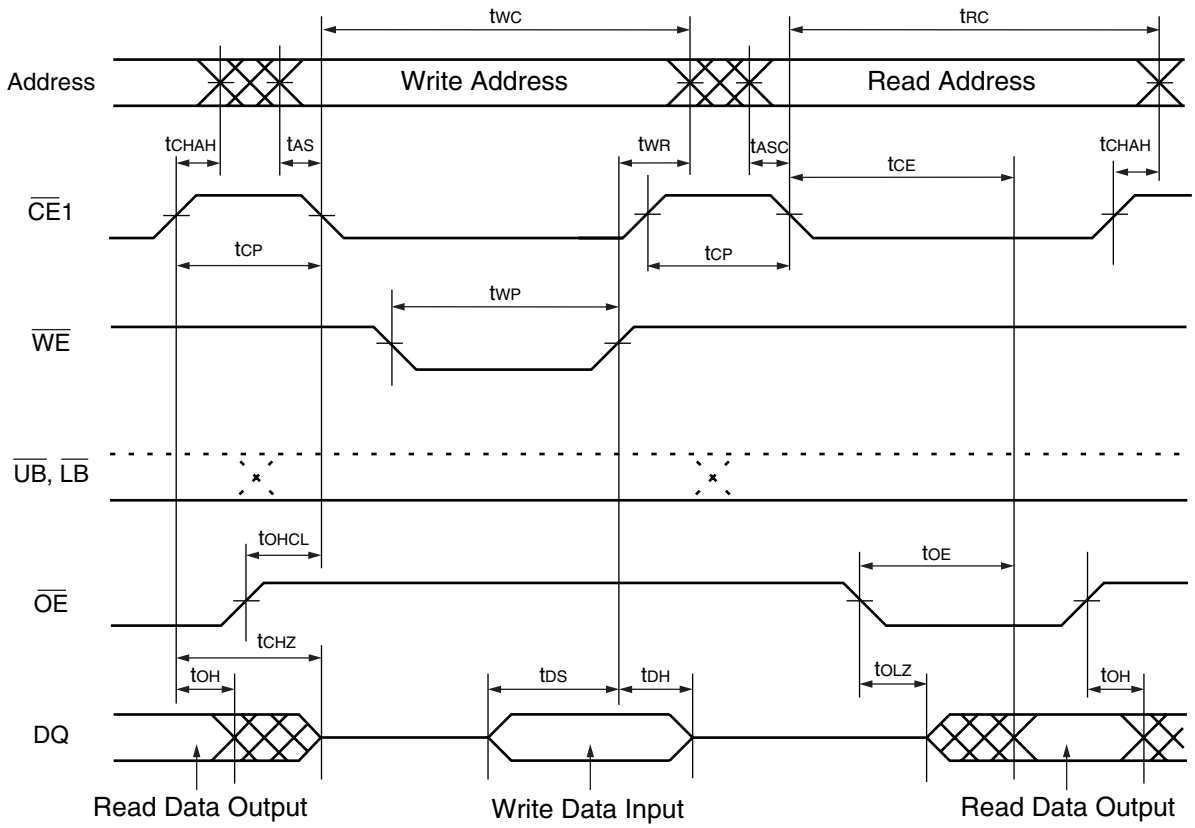
Note : This timing diagram assumes CE2 = H and $\overline{OE}$ = H.

(12) Read / Write Timing 1-1 ($\overline{CE}$1 Control)



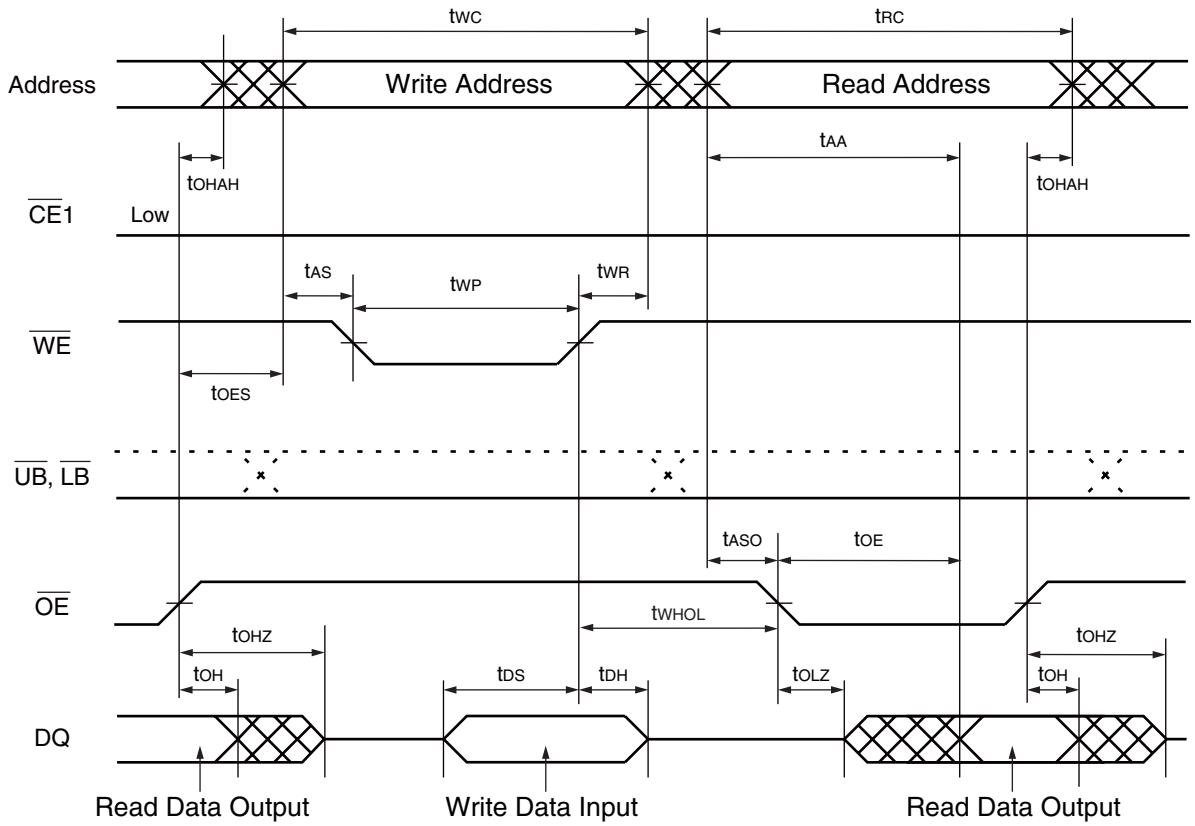
Notes : • This timing diagram assumes CE2 = H.
• Write address is valid from either $\overline{CE}$1 or $\overline{WE}$ of last falling edge.

(13) Read / Write Timing 1-2 ($\overline{CE}$1, $\overline{WE}$, $\overline{OE}$ Control)



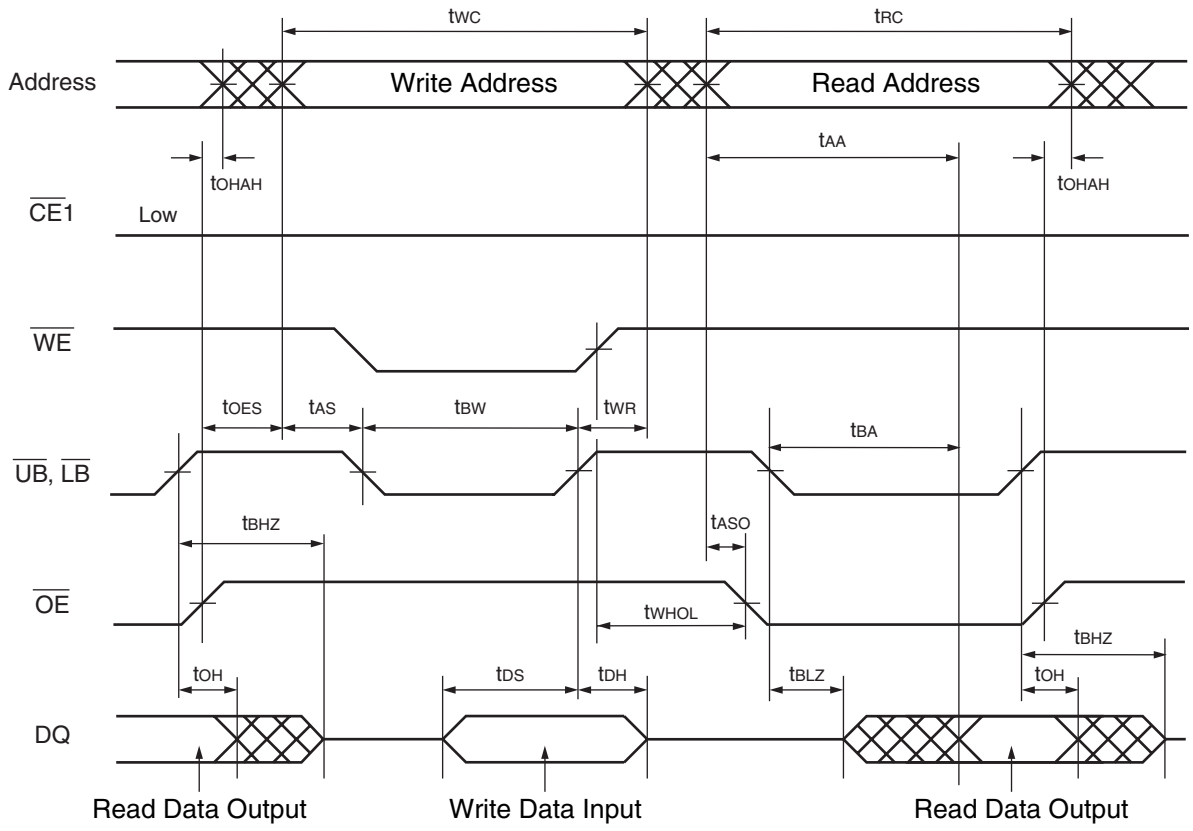
Notes : • This timing diagram assumes CE2 = H.
• $\overline{OE}$ can be fixed Low during write operation if it is $\overline{CE}$1 controlled write at Read-Write-Read sequence.

(14) Read / Write Timing 2 ($\overline{OE}$, $\overline{WE}$ Control)



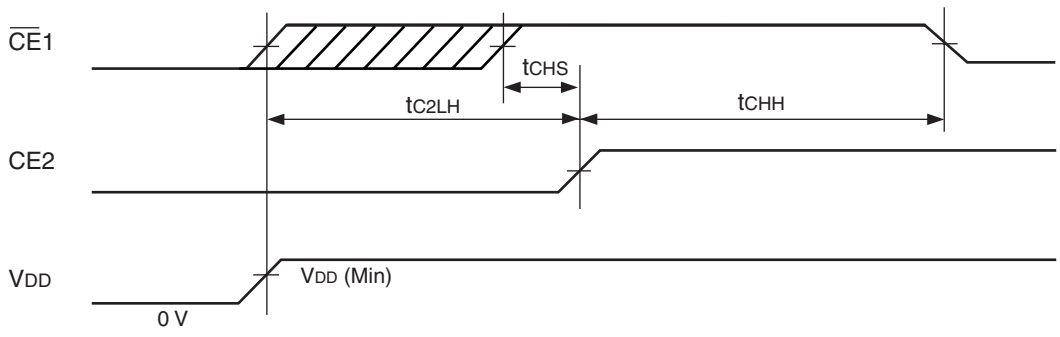
Notes : • This timing diagram assumes CE2 = H.
• $\overline{CE}$1 can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.

(15) Read / Write Timing 3 ($\overline{OE}$, $\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Control)



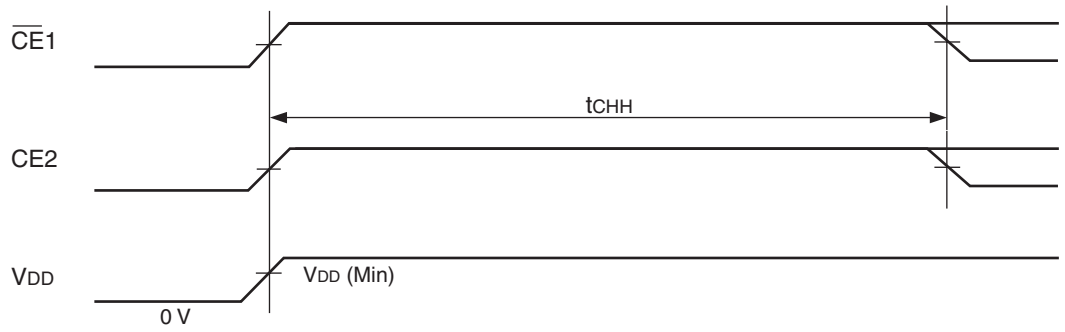
Notes : • This timing diagram assumes CE2 = H.
• $\overline{CE}$1 can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.
• Read data will be available after t_{AA} from $\overline{WE}$ = H if read address are not changed from write address.

(16) Power-up Timing 1



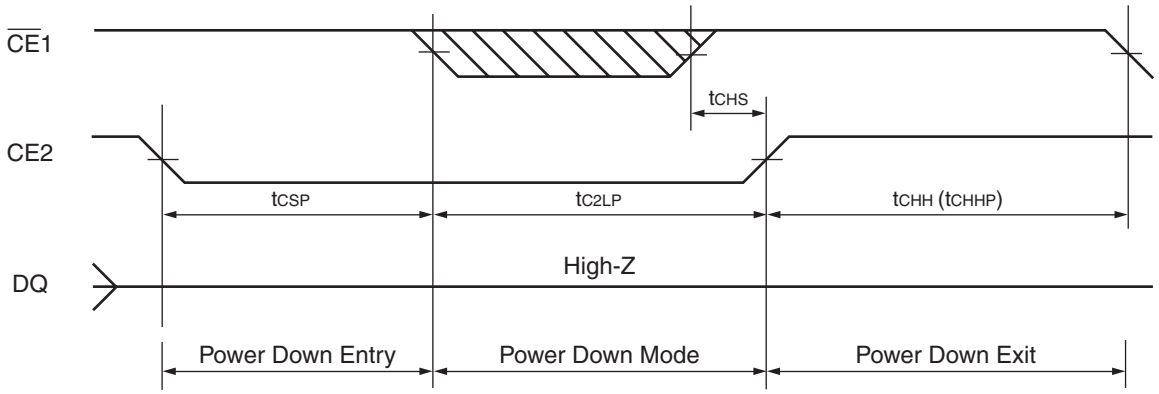
Note : The t_{C2LH} specifies after V_{DD} reaches specified minimum level.

(17) Power-up Timing 2



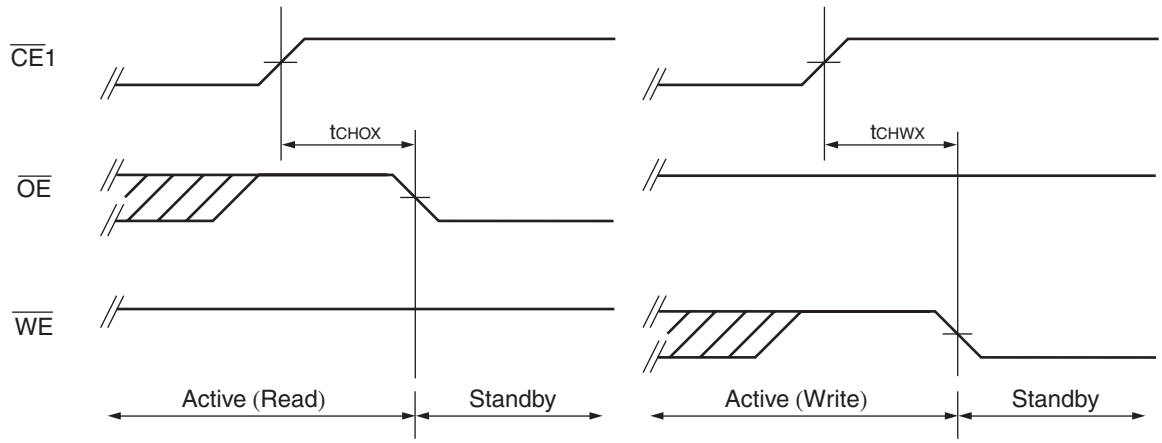
Note : The t_{CHH} specifies after V_{DD} reaches specified minimum level and applicable to both $\overline{CE}$1 and CE2. If transition time of V_{DD} (from 0 V to V_{DD} Min) is longer than 50 ms, " (16) Power-up Timing 1" must be applied.

(18) Power Down Entry and Exit Timing



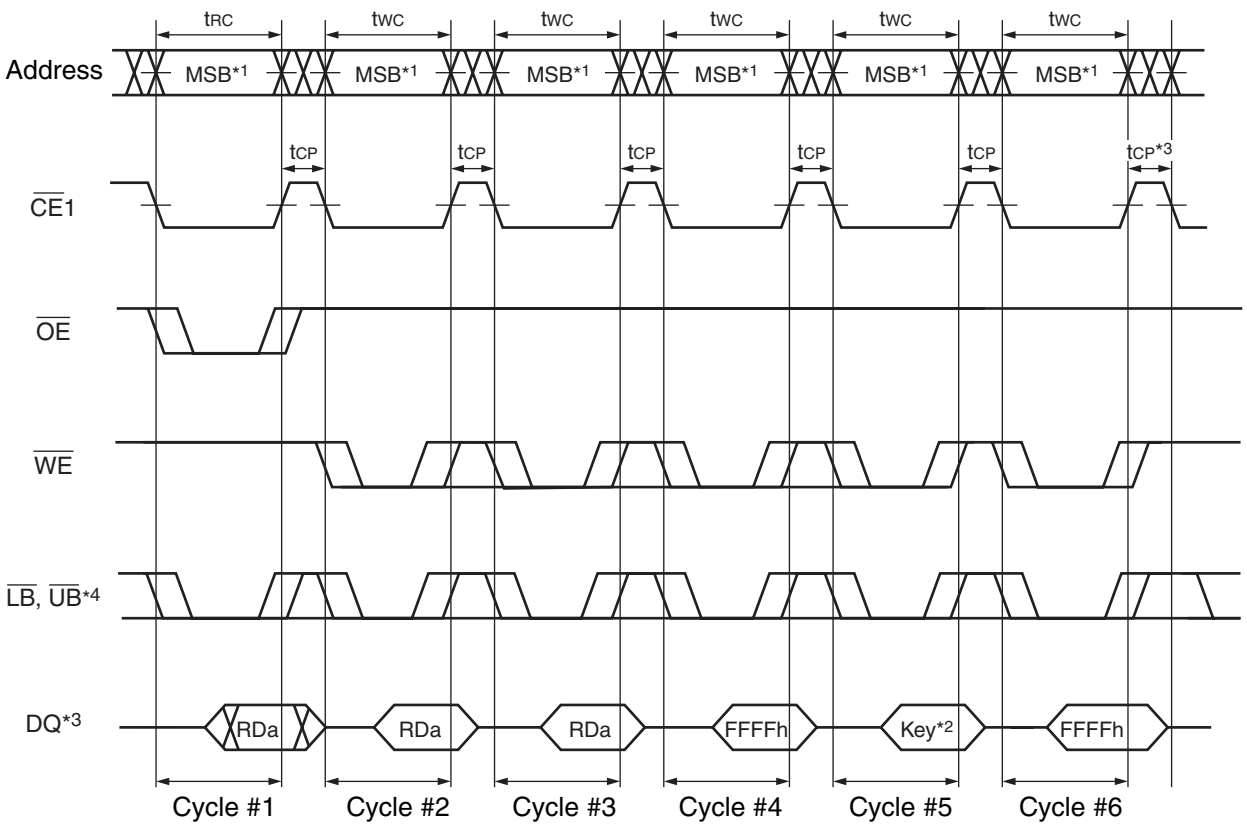
Notes : • This Power Down mode can be also used as a reset timing if "Power-up timing" above could not be satisfied and Power Down program was not performed prior to this reset.
• CE2 can be brought to Low after the completion of previous read/write operation.
• CE2 must be kept at High during the specified minimum time of t_{CP}.

(19) Standby Entry Timing after Read or Write



Note : Both t_{CHOX} and t_{CHWX} define the earliest entry timing for standby mode.

(20) Power Down Program Timing



*1 : The all address inputs must be High from Cycle #1 to #6.

*2 : The data key must conform to the format specified in "■ POWER DOWN". If not, the operation and data are not guaranteed.

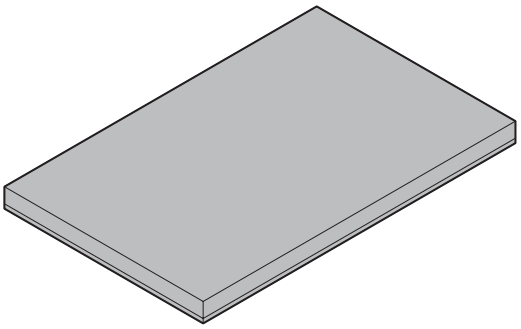
*3 : After t_{CP} following Cycle #6, the Power Down program is completed and returned to the normal operation.

*4 : Byte read or write is available in addition to word read or write. At least one byte control signal ($\overline{LB}$ or $\overline{UB}$) needs to be Low.

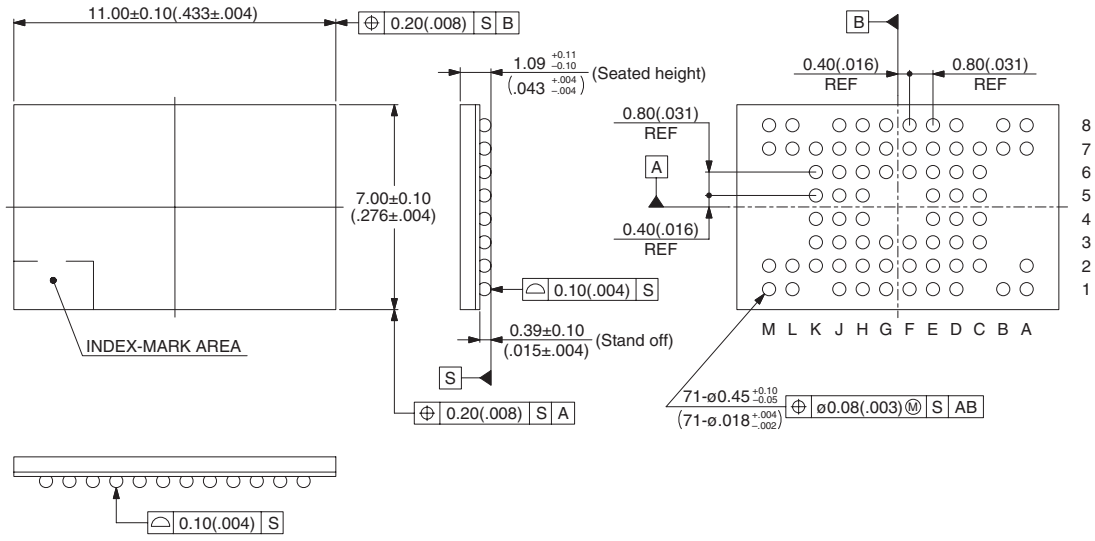
■ ORDERING INFORMATION

Part Number	Package
MB82DP04184E-65LTBG	71-ball plastic FBGA (BGA-71P-M03)

■ PACKAGE DIMENSION

71-ball plastic FBGA		
	Ball pitch	0.80 mm
	Package width × package length	7.00 × 11.00 mm
	Lead shape	Soldering ball
	Sealing method	Plastic mold
	Ball size	∅0.45 mm
	Mounting height	1.20 mm Max.
(BGA-71P-M03)	Weight	0.14 g

71-ball plastic FBGA
(BGA-71P-M03)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

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